**IN THE CLAIMS:**

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor device comprising:

~~a pixel portion comprising~~ a plurality of switching elements[[ and]];

a plurality of pixel electrodes;

an opposing electrode; and

a frame rate conversion portion, wherein:

an image signal is written into the frame rate conversion portion;

the image signal written is read out twice from the frame rate conversion portion;

the image signal which is read out twice from the frame rate conversion portion is then input to a source signal line driver circuit to make a display signal;

~~wherein a~~ the display signal is input to the plurality of pixel electrodes through the plurality of switching elements[[,]];

~~wherein~~ all of the display signals input to the plurality of pixel electrodes have the same polarity within each frame period, with the electric potential of the opposing electrode as a reference[[,]];

~~wherein~~ the frame rate conversion portion operates in synchronous with the display signals[[,]];

~~wherein~~ among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an

inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference[[,]]; and

~~wherein~~ a same image is displayed in a pixel portion in the two arbitrary, adjacent frame periods.

2. (Currently amended) A semiconductor device comprising:

~~a pixel portion comprising~~ a plurality of switching elements[[ and]];

a plurality of pixel electrodes;

an opposing electrode;

a plurality of source signal lines; and

a frame rate conversion portion, , wherein:

an image signal is written into the frame rate conversion portion;

the image signal written is read out twice from the frame rate conversion portion;

the image signal which is read out twice from the frame rate conversion portion is then input to a source signal line driver circuit to make a display signal;

~~wherein a~~ the display signal input to the plurality of source signal lines is then input to the plurality of pixel electrodes through the plurality of switching elements[[,]];

~~wherein~~ within each frame period, display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines which are adjacent to the plurality of source signal lines, and the display signals input to each of the plurality of source signal line have the same polarity, with the electric potential of the opposing electrode as a reference[[,]];

~~wherein~~ the frame rate conversion portion operates in synchronous with the display

signals[[,]];

~~wherein~~ among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference[[,]]; and

~~wherein~~ a same image is displayed in a pixel portion in the two arbitrary, adjacent frame periods.

3. (Currently amended) A semiconductor device comprising:

~~a pixel portion comprising~~ a plurality of switching elements[[ and]];

a plurality of pixel electrodes;

an opposing electrode;

a plurality of source signal lines; and

a frame rate conversion portion,

an image signal is written into the frame rate conversion portion;

the image signal written is read out twice from the frame rate conversion portion;

the image signal which is read out twice from the frame rate conversion portion is then input to a source signal line driver circuit to make a display signal;

~~wherein a~~ the display signal input to the plurality of source signal lines is then input to the plurality of pixel electrodes through the plurality of switching elements[[,]];

~~wherein~~ within each frame period, the display signals input to all of the plurality of source signal lines have the same polarity, with the electric potential of the opposing electrode as a reference[[,]];

~~wherein~~ the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference[[,]];

~~wherein~~ the frame rate conversion portion operates in synchronous with the display signals[[,]];

~~wherein~~ among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference[[,]]; and

~~wherein~~ a same image is displayed in a pixel portion in the two arbitrary, adjacent frame periods.

4. (Currently amended) A semiconductor device comprising:

~~a pixel portion comprising~~ a plurality of switching elements[[ and]];

a plurality of pixel electrodes;

an opposing electrode;

a plurality of source signal lines; and

a frame rate conversion portion,

an image signal is written into the frame rate conversion portion;

the image signal written is read out twice from the frame rate conversion portion;

the image signal which is read out twice from the frame rate conversion portion is then input to a source signal line driver circuit to make a display signal;

~~wherein a~~ the display signal input to the plurality of source signal lines is input to the

plurality of pixel electrodes through the plurality of switching elements[[,]];

~~wherein~~ within each frame period, display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines[[,]];

~~wherein~~ the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference[[,]];

~~wherein~~ the frame rate conversion portion operates in synchronous with the display signals[[,]];

~~wherein~~ among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference[[,]]; and

~~wherein~~ a same image is displayed in a pixel portion in the two arbitrary, adjacent frame periods.

5-15. (Canceled)

16. (Previously presented) A semiconductor display device according to any one of claims 1 to 15, wherein the switching element is: a transistor formed using single crystal silicon; a thin film transistor formed using polycrystalline silicon; or a thin film transistor formed using amorphous silicon.

17. (Previously presented) A computer using the semiconductor display device according to claims 1.

18. (Previously presented) A video camera using the semiconductor display device according to claim 1.

19. (Previously presented) A DVD player using the semiconductor display device according to claim 1.

20-24. (Canceled)

25. (Previously presented) A semiconductor device according to claim 2, wherein the switching element is: a transistor formed over using single crystal silicon; a thin film transistor formed using polycrystalline silicon; or a thin film transistor formed using amorphous silicon.

26. (Previously presented) A semiconductor device according to claim 3, wherein the switching element is: a transistor formed over using single crystal silicon; a thin film transistor formed using polycrystalline silicon; or a thin film transistor formed using amorphous silicon.

27. (Previously presented) A semiconductor device according to claim 4, wherein the switching element is: a transistor formed over using single crystal silicon; a thin film transistor formed using polycrystalline silicon; or a thin film transistor formed using amorphous silicon.

28-38. (Canceled)

39. (Previously presented) A computer using the semiconductor display device according to claim 1.

40. (Previously presented) A computer using the semiconductor display device according to claim 2.

41. (Previously presented) A computer using the semiconductor display device according to claim 3.

42. (Previously presented) A computer using the semiconductor display device according to claim 4.

43-47. (Canceled)

48. (Previously presented) A video camera using the semiconductor display device according to claim 1.

49. (Previously presented) A video camera using the semiconductor display device according to claim 2.

50. (Previously presented) A video camera using the semiconductor display device according to claim 3.

51. (Previously presented) A video camera using the semiconductor display device according to claim 4.

52-56. (Canceled)

57. (Previously presented) A DVD player using the semiconductor display device according to claim 1.

58. (Previously presented) A DVD player using the semiconductor display device according to claim 2.

59. (Previously presented) A DVD player using the semiconductor display device according to claim 3.

60. (Previously presented) A DVD player using the semiconductor display device according to claim 4.

61-65. (Canceled)

66. (New) A method of driving a display device comprising steps of:

writing an image signal into a frame rate conversion portion during a first period;

first reading out said image signal from said frame rate conversion portion during a second period;

second reading out said image signal from said frame rate conversion portion during said second period after said first reading;

sampling the first read out image signal and the second read out image signal by a source signal line driver circuit in order; and

supplying the sampled first image signal to a pixel portion in a first frame period and the sampled second image signal to said pixel portion in a second frame period after said first frame period wherein images displayed in said pixel portion in the first frame period and the second frame period are the same,

wherein a polarity of one of the first and second image signals is inverted before the first and second image signals are sampled by said source signal line driver circuit.

67. (New) The method of driving a display device according to claim 66, further comprising a step of writing a second image signal into the frame rate conversion portion during said second period.

68. (New) The method of driving a display device according to claim 66, wherein the image signal written into the frame rate conversion portion is a digital signal.

69. (New) The method of driving a display device according to claim 66, further comprising a step of performing a D/A conversion of the first read out image signal and the second read out image signal.